Systemc Golden Reference Guide

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With C and GNU Development Tools Springer Science & Business Media
'Downright revolutionary... the title is a major understatement... 'Quantum Programming' may ultimately change the way embedded software is designed.' -- Michael Barr, Editor-in-Chief, Embedded Systems Programming magazine (Click here
APPLYING UML & PATTERNS 3RD EDITION Springer
Larman covers how to investigate requirements, create solutions and then translate designs into code, showing developers how to make practical use of the most significant recent developments. A summary of UML notation is included
Advances in Network Security and Applications "O'Reilly Media, Inc."
Contributions on UML address the application of UML in the specification of embedded HW/SW systems. C-Based System Design embraces the modeling of operating systems, modeling with different models of computation, generation of test patterns, and experiences from case studies with SystemC. Analog and Mixed-Signal Systems covers rules for solving general modeling problems in VHDL-AMS, modeling of multi-nature systems, synthesis, and modeling of Mixed-Signal Systems with SystemC. Languages for formal methods are addressed by contributions on formal specification and refinement of hybrid, embedded and real-time stems. Together with articles on new languages such as SystemVerilog and Software Engineering in Automotive Systems the contributions selected for this book embrace all aspects of languages and models for specification, design, modeling and verification of systems. Therefore, the book gives an excellent overview of the actual state-of-the-art and the latest research results.
Methodology and Techniques Greenwood Publishing Group
This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on

the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

Languages for System Specification Springer Science & Business Media This book contains extended and revised versions of the best papers presented at the 22nd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2014, held in Playa del Carmen, Mexico, in October 2014. The 12 papers included in the book were carefully reviewed and selected from the 33 full papers presented at the conference. The papers cover a wide range of topics in VLSI technology and advanced research. They address the current trend toward increasing chip integration and technology process advancements bringing about stimulating new challenges both at the physical and system-design levels, as well as in the test of these systems.

14th International Conference , FPL 2004, Leuven, Belgium, August 30-September 1, 2004, Proceedings Springer Science & Business Media Digital Design: An Embedded Systems Approach Using Verilog provides a foundation in digital design for students in computer engineering, electrical engineering and computer science courses. It takes an up-to-date and modern approach of presenting digital logic design as an activity in a larger systems design context. Rather than focus on aspects of digital design that have little relevance in a realistic design context, this book concentrates on modern and evolving knowledge and design skills. Hardware description language (HDL)-based design and verification is emphasized--Verilog examples are used extensively throughout. By treating digital logic as part of embedded systems design, this book provides an understanding of the hardware needed in the analysis and design of systems comprising both hardware and software components. Includes a Web site with links to vendor tools, labs and tutorials. Presents digital logic design as an activity in a larger systems design context Features extensive use of Verilog examples to demonstrate HDL (hardware description language) usage at the abstract behavioural level and register transfer level, as well as for low-level verification and verification environments Includes worked examples throughout to enhance the reader's understanding and retention of the material Companion Web site includes links to tools for FPGA design from Synplicity, Mentor Graphics, and Xilinx, Verilog source code for all the examples in the book, lecture slides, laboratory projects, and solutions to exercises

Entwurf, Modellierung und Synthese Springer Science & Business Media This book constitutes the proceedings of the 4th

International Conference on Network Security and Applications held in Chennai, India, in July 2011. The 63 revised full papers presented were carefully reviewed and selected from numerous submissions. The papers address all technical and practical aspects of security and its applications for wired and wireless networks and are organized in topical sections on network security and applications, ad hoc, sensor and ubiquitous computing, as well as peer-to-peer networks and trust management.

SystemC: From the Ground Up Oldenbourg Verlag

Authored by two of the leading authorities in the field, this guide offers readers the knowledge and skills needed to achieve proficiency with embedded software.

A Practical Approach to VLSI System on Chip (SoC) Design Universal-Publishers

Offers users the first resource guide that combines both the methodology and basics of SystemVerilog Addresses how all these pieces fit together and how they should be used to verify complex chips rapidly and thoroughly. Unique in its broad coverage of SystemVerilog, advanced functional verification, and the combination of the two.

Practical Statecharts in C/C++ Elsevier

Silicon technology now allows us to build chips consisting of tens of millions of transistors. This technology not only promises new levels of system integration onto a single chip, but also presents significant challenges to the chip designer. As a result, many ASIC developers and silicon vendors are re-examining their design methodologies, searching for ways to make effective use of the huge numbers of gates now available. These designers see current design tools and methodologies as inadequate for developing million-gate ASICs from scratch. There is considerable pressure to keep design team size and design schedules constant even as design complexities grow. Tools are not providing the productivity gains required to keep pace with the increasing gate counts available from deep submicron technology. Design reuse - the use of pre-designed and pre-verified cores - is the most promising opportunity to bridge the gap between available gate-count and designer productivity. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition outlines an effective methodology for creating reusable designs for use in a System-on-a-Chip (SoC) design methodology. Silicon and tool technologies move so quickly that no single methodology can provide a permanent solution to this highly dynamic problem. Instead, this manual is an attempt to capture and incrementally improve on current best practices in the industry, and to give a coherent, integrated view of the design process. Reuse Methodology Manual for System-On-A-Chip Designs, Second Edition will be updated on a regular basis as a result of changing technology and improved insight into the problems of design reuse and its role in producing high-quality SoC designs.

A Roadmap for Formal Property Verification Twayne Publishers

This book contains the papers presented at the 14th International Conference on Field Programmable Logic and Applications (FPL) held

during August 30th-September 1st 2004. The conference was hosted by the Interuniversity Micro-Electronics Center (IMEC) in Leuven, Belgium. The FPL series of conferences was founded in 1991 at Oxford University (UK), and has been held annually since: in Oxford (3 times), Vienna, Prague, Darmstadt, London, Tallinn, Glasgow, Villach, Belfast, Montpellier and Lisbon. It is the largest and oldest conference in reconfigurable computing and brings together academic researchers, industry experts, users and newcomers in an informal, welcoming atmosphere that encourages productive exchange of ideas and knowledge between the delegates. The fast and exciting advances in field programmable logic are increasing steadily with more and more application potential and need. New ground has been broken in architectures, design techniques, (partial) run-time reconfiguration and applications of field programmable devices in several different areas. Many of these recent innovations are reported in this volume. The size of the FPL conferences has grown significantly over the years. FPL in 2003 saw 216 papers submitted. The interest and support for FPL in the programmable logic community continued this year with 285 scientific papers submitted, demonstrating a 32% increase when compared to the year before. The technical program was assembled from 78 selected regular papers, 45 additional short papers and 29 posters, resulting in this volume of proceedings. The program also included three invited plenary keynote presentations from Xilinx, Gilder Technology Report and Altera, and three embedded tutorials from Xilinx, the Universit¨ at Karlsruhe (TH) and the University of Oslo.

Languages, Design Methods, and Tools for Electronic System Design

"O'Reilly Media, Inc."

Dieses Buch ist eine Einführung in die wichtigsten Themen und Fragestellungen beim Entwurf von Eingebetteten und Cyber-Physischen Systemen. Ausgehend von den zugrundeliegenden Technologien, Prozessor- und Netzwerkarchitekturen werden Modellierungssprachen und moderne Ansätze zur Analyse und Synthese von eingebetteten Hardware/Software-Systemen vorgestellt. Einen breiten Raum nimmt das Gebiet Entwicklungsmethodik ein, das für Studierende sowie Informatiker und Ingenieure gedacht ist, die als Entwickler tätig werden wollen oder es bereits sind. Der Stoff wird anschaulich anhand vieler Bilder und Beispiele dargestellt. Dabei verzichten wir bewusst auf mathematische Beweise und Formalismen und setzen den Fokus auf die Darstellung aktueller Methoden und Ansätze aus Wissenschaft und Industrie mit hoher Praxisrelevanz. Somit kann der Text auch als Ergänzung für eine formalere Behandlung des Themas verwendet werden. Das Werk orientiert sich didaktisch an einer zweisemestrigen Vorlesung im Masterstudiengang der Universität Tübingen. Einzelne Kapitel können als getrennte Vorlesungseinheiten verwendet werden.

Verification Methodology Manual for SystemVerilog

Springer Science & Business Media

SystemC provides a robust set of extensions

to C++ that enables rapid development of complex hardware/software systems. This book focuses on the practical uses of the language for modeling real systems. The wealth of examples and downloadable code methodically guide the reader through the finer points of the SystemC language. This work provides: - A step-by-step build-up of syntax - NEW features of SystemC 2.1 - Code examples for each concept, - Many resource references - Coding styles and guidelines - Over 52 downloadable code examples (over 8,000 lines) - Exercises throughout the book - How SystemC fits into the system design methodology - Why features are as they are Well known consultants in the EDA industry, both David Black and Jack Donovan have been involved in the adoption and teaching of new technologies and methodologies for a combined total of 42+ years. Recently, they jointly founded a consultancy, Eklectic Ally, focused on helping companies adopt SystemC methodologies.

Electronic Design John Wiley & Sons

The book is designed to serve as a textbook for courses offered to graduate and undergraduate students enrolled in electronics and electrical engineering and computer science. This book attempts to bridge the gap between electronics and computer science students, providing complementary knowledge that is essential for designing an embedded system. The book covers key concepts tailored for embedded system design in one place. The topics covered in this book are models and architectures, Executable Specific Languages – SystemC, Unified Modeling Language, real-time systems, real-time operating systems, networked embedded systems, Embedded Processor architectures, and platforms that are secured and energy-efficient. A major segment of embedded systems needs hard real-time requirements. This textbook includes real-time concepts including algorithms and real-time operating system standards like POSIX threads. Embedded systems are mostly distributed and networked for deterministic responses. The book covers how to design networked embedded systems with appropriate protocols for real-time requirements. Each chapter contains 2-3 solved case studies and 10 real-world problems as exercises to provide detailed coverage and essential pedagogical tools that make this an ideal textbook for students enrolled in electrical and electronics engineering and computer science programs.

An Embedded Systems Approach Using Verilog Springer Science & Business Media

Functional verification is an art as much as a science. It requires not only creativity and cunning, but also a clear methodology to approach the problem. The Open Verification Methodology (OVM) is a leading-edge methodology for verifying designs at multiple levels of abstraction. It brings together ideas from electrical, systems, and software engineering to provide a complete methodology for verifying large scale System-on-Chip (SoC) designs. OVM defines an approach for developing testbench architectures so they are modular, configurable, and reusable. This book is designed to help both

novice and experienced verification engineers master the OVM through extensive examples. It describes basic verification principles and explains the essentials of transaction-level modeling (TLM). It leads readers from a simple connection of a producer and a consumer through complete self-checking testbenches. It explains construction techniques for building configurable, reusable testbench components and how to use TLM to communicate between them. Elements such as agents and sequences are explained in detail.

Transaction-Level Modeling with SystemC Springer Nature

The IFIP TC-10 Working Conference on Distributed and Parallel Embedded Systems (DIPES 2004) brings together experts from industry and academia to discuss recent developments in this important and growing field in the splendid city of Toulouse, France. The ever decreasing price/performance ratio of microcontrollers makes it economically attractive to replace more and more conventional mechanical or electronic control systems within many products by embedded real-time computer systems. An embedded real-time computer system is always part of a well-specified larger system, which we call an intelligent product. Although most intelligent products start out as stand-alone units, many of them are required to interact with other systems at a later stage. At present, many industries are in the middle of this transition from stand-alone products to networked embedded systems. This transition requires reflection and architecting: The complexity of the evolving distributed artifact can only be controlled, if careful planning and principled design methods replace the - hoc engineering of the first version of many standalone embedded products.

Design Methods and Applications for Distributed Embedded Systems Elsevier

mental improvements during the same period. What is clearly needed in verification techniques and technology is the equivalent of a synthesis productivity breakthrough. In the second edition of Writing Testbenches, Bergeron raises the verification level of abstraction by introducing coverage-driven constrained-random transaction-level self-checking testbenches all made possible through the introduction of hardware verification languages (HVLs), such as e from Verisity and OpenVera from Synopsys. The state-of-art methodologies described in Writing Test benches will contribute greatly to the much-needed equivalent of a synthesis breakthrough in verification productivity. I not only highly recommend this book, but also I think it should be required reading by anyone involved in design and verification of today's ASIC, SoCs and systems. Harry Foster Chief Architect Verplex Systems, Inc. xviii Writing Testbenches: Functional Verification of HDL Models PREFACE If you survey hardware design groups, you will learn that between 60% and 80% of their effort is now dedicated to verification.

Devices, Tools and Flows Springer Science & Business Media

If you’re just learning how to program, Julia is an excellent JIT-compiled, dynamically typed language with a clean

syntax. This hands-on guide uses Julia 1.0 to walk you through programming one step at a time, beginning with basic programming concepts before moving on to more advanced capabilities, such as creating new types and multiple dispatch. Designed from the beginning for high performance, Julia is a general-purpose language ideal for not only numerical analysis and computational science but also web programming and scripting. Through exercises in each chapter, you'll try out programming concepts as you learn them. Think Julia is perfect for students at the high school or college level as well as self-learners and professionals who need to learn programming basics. Start with the basics, including language syntax and semantics Get a clear definition of each programming concept Learn about values, variables, statements, functions, and data structures in a logical progression Discover how to work with files and databases Understand types, methods, and multiple dispatch Use debugging techniques to fix syntax, runtime, and semantic errors Explore interface design and data structures through case studies

Advanced Verification Techniques Xlibris Corporation

Are you an RTL or system designer that is currently using, moving, or planning to move to an HLS design environment? Finally, a comprehensive guide for designing hardware using C++ is here. Michael Fingeroff's High-Level Synthesis Blue Book presents the most effective C++ synthesis coding style for achieving high quality RTL. Master a totally new design methodology for coding increasingly complex designs! This book provides a step-by-step approach to using C++ as a hardware design language, including an introduction to the basics of HLS using concepts familiar to RTL designers. Each chapter provides easy-to-understand C++ examples, along with hardware and timing diagrams where appropriate. The book progresses from simple concepts such as sequential logic design to more complicated topics such as memory architecture and hierarchical sub-system design. Later chapters bring together many of the earlier HLS design concepts through their application in simplified design examples. These examples illustrate the fundamental principles behind C++ hardware design, which will translate to much larger designs. Although this book focuses primarily on C and C++ to present the basics of C++ synthesis, all of the concepts are equally applicable to SystemC when describing the core algorithmic part of a design. On completion of this book, readers should be well on their way to becoming experts in high-level synthesis.

For System-on-a-Chip Designs Intl. Engineering Consortiu

The first edition of Principles of Verifiable RTL Design offered a common sense method for simplifying and unifying assertion specification by creating a set of predefined specification modules that could be instantiated within the designer's RTL. Since the release of the first edition, an entire industry-wide initiative for assertion specification has emerged based on ideas presented in the first edition. This initiative, known as the Open Verification Library

Initiative (www.verificationlib.org), provides an assertion interface standard that enables the design engineer to capture many interesting properties of the design and precludes the need to introduce new HDL constructs (i.e., extensions to Verilog are not required). Furthermore, this standard enables the design engineer to `specify once,' then target the same RTL assertion specification over multiple verification processes, such as traditional simulation, semi-formal and formal verification tools. The Open Verification Library Initiative is an empowering technology that will benefit design and verification engineers while providing unity to the EDA community (e.g., providers of testbench generation tools, traditional simulators, commercial assertion checking support tools, symbolic simulation, and semi-formal and formal verification tools). The second edition of Principles of Verifiable RTL Design expands the discussion of assertion specification by including a new chapter entitled `Coverage, Events and Assertions'. All assertions exampled are aligned with the Open Verification Library Initiative proposed standard. Furthermore, the second edition provides expanded discussions on the following topics: start-up verification; the place for 4-state simulation; race conditions; RTL-style-synthesizable RTL (unambiguous mapping to gates); more `bad stuff'. The goal of the second edition is to keep the topic current. Principles of Verifiable RTL Design, A Functional Coding Style Supporting Verification Processes, Second Edition tells you how you can write Verilog to describe chip designs at the RTL level in a manner that cooperates with verification processes. This cooperation can return an order of magnitude improvement in performance and capacity from tools such as simulation and equivalence checkers. It reduces the labor costs of coverage and formal model checking by facilitating communication between the design engineer and the verification engineer. It also orients the RTL style to provide more useful results from the overall verification process.