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P2. Designing multiplexers using VHDL. Eight channel multiplexer (MUX_8). Plan A: structural (SoP) **VHDL Lecture 3 Lab1 Switches LEDs Explanation VHDL Basics** 10.4(a) Modeling ROM in VHDL Reduction of state table by the method of Implication chart | Logic Circuit design **EEVblog #635**

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