Chip Package Co Design Of Integrated Mixed Signal Systems

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Chip Package Co Design Of Integrated Mixed Signal Systems *2023-03-05*

MIGUEL COLON

Integrated Interconnect Technologies for 3D Nanoelectronic Systems Springer
This book describes methods for distributing power in high speed, high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt. It provides a broad and cohesive treatment of power distribution systems and related design problems, including both circuit network models and design techniques for on-chip decoupling capacitors, providing insight and intuition into the behavior and design of on-chip power distribution systems. Organized into subareas to provide a more intuitive flow to the reader, this second edition adds more than a hundred pages of new content, including inductance models for interdigitated structures, design strategies for multi-layer power grids, advanced methods for efficient power grid design and analysis, and methodologies for simultaneously placing on-chip multiple power supplies and decoupling capacitors. The emphasis of this additional material is on managing the complexity of on-chip power distribution networks.
New Vistas on Concurrent Engineering Chip-package Codesign Springer
This book is the first standalone book that combines research into low-noise amplifiers (LNAs) with research into millimeter-wave circuits. In compiling this book, the authors have set two research objectives. The first is to bring together the research context behind millimeter-wave circuit operation and the theory of low-noise amplification. The second is to present new research in this multi-disciplinary field by dividing the common LNA configurations and typical specifications into subsystems, which are then optimized separately to suggest improvements in the current state-of-the-art designs. To achieve the second research objective, the state-of-the-art LNA configurations are discussed and the weaknesses of state-of the art configurations are considered, thus identifying research gaps. Such research gaps, among others, point towards optimization – at a systems and microelectronics level. Optimization topics include the influence of short wavelength, layout and crosstalk on LNA performance. Advanced fabrication technologies used to decrease the parasitics of passive and active devices are also explored, together with packaging technologies such as silicon-on-chip and silicon-on-package, which are proposed as alternatives to traditional IC implementation. This research outcome builds through innovation. Innovative ideas for LNA construction are explored, and alternative design methodologies are deployed, including LNA/antenna co-design or utilization of the electronic design automation in the research flow. The book also offers the authors' proposal for streamlined automated LNA design flow, which focuses on LNA as a collection of highly optimized subsystems.
Systems for Ubiquitous Tagging Newnes
This book explains for readers how 3D chip stacks promise to increase the level of on-chip integration, and to design new heterogeneous semiconductor devices that combine chips of different integration technologies (incl. sensors) in a single package of the smallest possible size. The authors focus on heterogeneous 3D integration, addressing some of the most important challenges in this emerging technology, including contactless, optics-based, and carbon-nanotube-based 3D integration, as well as signal-integrity and thermal management issues in copper-based 3D integration. Coverage also includes the 3D heterogeneous integration of power sources, photonic devices, and non-volatile memories based on new materials systems.
CPD'98 : ETH Zürich, Switzerland, March 24-26 1998 Springer Science & Business Media
Advanced Packaging serves the semiconductor packaging, assembly and test industry. Strategically focused on emerging and leading-edge methods for manufacturing and use of advanced packages.
Power Distribution Networks in High Speed Integrated Circuits Springer Science & Business Media
This book provides readers with a variety of algorithms and software tools, dedicated to the physical design of through-silicon-via (TSV) based, three-dimensional integrated circuits. It describes numerous "manufacturing-ready" GDSII-level layouts of TSV-based 3D ICs developed with the tools covered in the book. This book will also feature sign-off level analysis of timing, power, signal integrity, and thermal analysis for 3D IC designs. Full details of the related algorithms will be provided so that the readers will be able not only to grasp the core mechanics of the physical design tools, but also to be able to reproduce and improve upon the results themselves. This book will also offer various design-for-manufacturability (DFM), design-for-reliability (DFR), and design-for-testability (DFT) techniques that are considered critical to the physical design process.
In-situ Characterization of High Speed I/O Chip-package Systems John Wiley & Sons
Distributing power in high speed, high complexity integrated circuits has become a challenging task as power levels exceeding tens of watts have become commonplace while the power supply is plunging toward one volt. This book is dedicated to this important subject. The primary purpose of this monograph is to provide insight and intuition into the behavior and design of power distribution systems for high speed, high complexity integrated circuits.
Electrical and Layout Perspectives Second International Workshop on Chip Package Co-designInternational Workshop on Chip Package Co-designNew Vistas on Concurrent Engineering Chip-package CodesignSummary IEEE International Workshop on Chip- Package Co-Design : CPD'98Power Distribution Network Design for VLSI
A modern, comprehensive introduction to DRAM for students and practicing chip designers Dynamic Random Access Memory (DRAM) technology has been one of the greatestdriving forces in the advancement of solid-state technology. With its ability to produce high product volumes and low pricing, it forces solid-state memory manufacturers to work aggressively to cut costs while maintaining, if not increasing, their market share. As a result, the state of the art continues to advance owing to the tremendous pressure to get more memory chips from each silicon wafer, primarily through process scaling and clever design. From a team of engineers working in memory circuit design, DRAM Circuit Design gives students and practicing chip designers an easy-to-follow, yet thorough, introductory treatment of the subject. Focusing on the chip designer rather than the end user, this volume offers expanded, up-to-date coverage of DRAM circuit design by presenting both standard and high-speed implementations. Additionally, it explores a range of topics: the DRAM array, peripheral circuitry, global circuitry and considerations, voltage converters, synchronization in DRAMs, data path design, and power delivery. Additionally, this up-to-date and comprehensive book features topics in high-speed design and architecture and the ever-increasing speed requirements of memory circuits. The only book that covers the breadth and scope of the subject under one cover, DRAM Circuit Design is an invaluable introduction for students in courses on memory circuit design or advanced digital courses in VLSI or CMOS circuit design. It also serves as an essential, one-stop resource for academics, researchers, and practicing engineers.
Chip and Package Co-design for Colpitts Oscillators Bentham Science Publishers
Three-Dimensional Integrated Circuit Design, Second Eition, expands the original with more than twice as much new content, adding the latest developments in circuit models, temperature considerations, power management, memory issues, and heterogeneous integration. 3-D IC experts Pavlidis, Savidis, and Friedman cover the full product development cycle throughout the book, emphasizing not only physical design, but also algorithms and system-level considerations to increase speed while conserving energy. A handy, comprehensive reference or a practical design guide, this book provides effective solutions to specific challenging problems concerning the design of three-dimensional integrated circuits. Expanded with new chapters and updates throughout based on the latest research in 3-D integration: Manufacturing techniques for 3-D ICs with TSVs Electrical modeling and closed-form expressions of through silicon vias Substrate noise coupling in heterogeneous 3-D ICs Design of 3-D ICs with inductive links Synchronization in 3-D ICs Variation effects on 3-D ICs Correlation of WID variations for intra-tier buffers and wires Offers practical guidance on designing 3-D heterogeneous systems Provides power delivery of 3-D ICs Demonstrates the use of 3-D ICs within heterogeneous systems that include a variety of materials, devices, processors, GPU-CPU integration, and more Provides experimental case studies in power delivery, synchronization, and thermal characterization
A Design Flow for Power Stripes and Micro Bumps Planning on Modern Chip-Package Co-Design Wiley-VCH
ABSTRACT: The evolution of high speed digital buses is pushing interface speeds up to frequencies of a few GHz making it difficult to create a working digital system in one design cycle and meeting the target time-to-market. With more functionality on the chip, designers have to cope with higher I/O densities, more signals coming out of a chip and tighter geometries. These higher performance requirements have a significant negative impact on system signal integrity. Thus, high-speed circuit and I/O designers cannot predict exactly what will happen after a chip is integrated with a package and a board. The influence of the package on the system performance must be understood and analyzed early in the design cycle and chip-package co-design is becoming essential to achieve time-to-market goal. In the chip-package co-design trends, it's important to construct and validate accurate modeling of the package and the PCB over tens of GHz frequency bandwidths. Conventional ways to model the package depend on the input from three dimensional full-wave EM solvers, two dimensional planar EM solvers, VNA, or TDR. Conventional solutions require excessive computation time (3-D solver) over simplification of the EM physics (2-D solver) or excessive characterization resources and time (VNA and TDR).
Chipless and Conventional Radio Frequency Identification: Systems for Ubiquitous Tagging CRC Press
This book describes methods for distributing power in high speed, high complexity integrated circuits with power levels exceeding many tens of watts and power supplies below a volt. It provides a broad and cohesive treatment of power delivery and management systems and related design problems, including both circuit network models and design techniques for on-chip decoupling capacitors, providing insight and intuition into the behavior and design of on-chip power distribution systems. Organized into subareas to provide a more intuitive flow to the reader, this fourth edition adds more than a hundred pages of new content, including inductance models for interdigitated structures, design strategies for multi-layer power grids, advanced methods for efficient power grid design and analysis, and methodologies for simultaneously placing on-chip multiple power supplies and decoupling capacitors. The emphasis of this additional material is on managing the complexity of on-chip power distribution networks.
From Emerging Processes to Heterogeneous Systems CRC Press
"The last couple of years have been very busy for the semiconductor industry and researchers. The rapid speed of production channel length reduction has brought lithographic challenges to semiconductor modeling. These include stress optimization, transisto"
Routing Algorithms for Chip-package-board Co-design Springer Science & Business Media
Issues in Computer Programming / 2011 Edition is a ScholarlyEditions™ eBook that delivers timely, authoritative, and comprehensive information about Computer Programming. The editors have built Issues in Computer Programming: 2011 Edition on the vast information databases of ScholarlyNews.™ You can expect the information about Computer Programming in this eBook to be deeper than what you can access anywhere else, as well as consistently reliable, authoritative, informed, and relevant. The content of Issues in Computer Programming: 2011 Edition has been produced by the world's leading scientists, engineers, analysts, research institutions, and companies. All of the content is from peer-reviewed sources, and all of it is written, assembled, and edited by the editors at ScholarlyEditions™ and available exclusively from us. You now have a source you can cite with authority, confidence, and credibility. More information is available at http://www.ScholarlyEditions.com/.
3D IC and RF SiPs: Advanced Stacking and Planar Solutions for 5G Mobility John Wiley &

Sons
The objective of this dissertation is to derive a set of compact physical models addressing power integrity issues in high performance gigascale integration (GSI) systems and three-dimensional (3-D) systems. The aggressive scaling of CMOS integrated circuits makes the design of power distribution networks a serious challenge. This is because the supply current and clock frequency are increasing, which increases the power supply noise. The scaling of the supply voltage slowed down in recent years, but the logic on the integrated circuit (IC) still becomes more sensitive to any supply voltage change because of the decreasing clock cycle and therefore noise margin. Excessive power supply noise can lead to severe degradation of chip performance and even logic failure. Therefore, power supply noise modeling and power integrity validation are of great significance in GSI systems and 3-D systems. Compact physical models enable quick recognition of the power supply noise without doing dedicated simulations. In this dissertation, accurate and compact physical models for the power supply noise are derived for power hungry blocks, hot spots, 3-D chip stacks, and chip/package co-design. The impacts of noise on transmission line performance are also investigated using compact physical modeling schemes. The models can help designers gain sufficient physical insights into the complicated power delivery system and tradeoff various important chip and package design parameters during the early stages of design. The models are compared with commercial tools and display high accuracy.

Ambient Intelligence with Microsystems IGI Global

Low Power Design Methodologies presents the first in-depth coverage of all the layers of the design hierarchy, ranging from the technology, circuit, logic and architectural levels, up to the system layer. The book gives insight into the mechanisms of power dissipation in digital circuits and presents state of the art approaches to power reduction. Finally, it introduces a global view of low power design methodologies and how these are being captured in the latest design automation environments. The individual chapters are written by the leading researchers in the area, drawn from both industry and academia. Extensive references are included at the end of each chapter. Audience: A broad introduction for anyone interested in low power design. Can also be used as a text book for an advanced graduate class. A starting point for any aspiring researcher.

Power Distribution Network Design for VLSI Springer Science & Business Media

Surveys the electrical and layout perspectives of System-in-Package, the system integration technology that has emerged as a required technology to reduce the system board space and height in addition to the overall time-to-market and design cost of consumer electronics products such as those of cell phones, audio/video players and digital cameras.

Summary IEEE International Workshop on Chip- Package Co-Design : CPD'98 Springer Science & Business Media

Second International Workshop on Chip Package Co-designInternational Workshop on Chip Package Co-designNew Vistas on Concurrent Engineering Chip-package CodesignSummary IEEE International Workshop on Chip- Package Co-Design : CPD'98Power Distribution Network Design for VLSIJohn Wiley & Sons

Chip and Package Co-design for Mixed-signal Systems: SoC Versus SoP Springer

The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC System Design, Verification, and Testing thoroughly examines system-level design, microarchitectural design, logic verification, and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools, using performance metrics to select microprocessor cores for integrated circuit (IC) designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on high-level synthesis, system-on-chip (SoC) block-based design, and back-annotating system-level models Offering improved depth and modernity, Electronic Design Automation for IC System Design, Verification, and Testing provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals.

Electrical Design of Through Silicon Via CRC Press

A hands-on troubleshooting guide for VLSI network designers The primary goal in VLSI (very large scale integration) power network design is to provide enough power lines across a chip to reduce voltage drops from the power pads to the center of the chip. Voltage drops caused by the power network's metal lines coupled with transistor switching currents on the chip cause power supply noises that can affect circuit timing and performance, thus providing a constant challenge for designers of high-performance chips. Power Distribution Network Design for VLSI provides detailed information on this critical component of circuit design and physical integration for high-speed chips. A vital tool for professional engineers (especially those involved in the use of commercial tools), as well as graduate students of engineering, the text explains the design issues, guidelines, and CAD tools for the power distribution of the VLSI chip and package, and provides numerous examples for its effective application. Features of the text include: * An introduction to power distribution network design * Design perspectives, such as power network planning, layout specifications, decoupling capacitance insertion, modeling, and analysis * Electromigration phenomena * IR drop analysis methodology * Commands and user interfaces of the VoltageStorm(TM) CAD tool * Microprocessor design examples using on-chip power distribution * Flip-chip and package design issues * Power network measurement techniques from real silicon The author includes several case studies and a glossary of key words and basic terms to help readers understand and integrate basic concepts in VLSI design and power distribution.

Volume 4: Design, Test, and Thermal Management Artech House

"The chip-package interaction for a low voltage operational transconductance amplifier (OTA) is described in this thesis."--Abstract.

International Workshop on Chip Package Co-design ScholarlyEditions

This work is a comprehensive experimental investigation of chip to package wirebond interconnects for chip-package co-design. Wirebonds are interconnect bottlenecks in RF design, but are difficult to avoid due to their low cost and manufacturing ease. We have shown measurements on wirebonds in coplanar configuration with different return paths and also the cross coupling. We have also extracted lumped and distributed models and demonstrate the excellent agreement with measurements atleast upto 15GHz. We have proposed multi-wirebonds as a potential solution for better impedance matching. Different types of inductors with Q-factors of upto 100 have also been illustrated. We show influence of encapsulant on wirebonds and finally we also demonstrate a methodology to extract the time-domain response from S-parameters.